UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,164	07/30/2003	Kiran R. Desai	INTEL/17479	7644

34431 7590 11/23/2005

HANLEY, FLIGHT & ZIMMERMAN, LLC
20 N. WACKER DRIVE
SUITE 4220
CHICAGO, IL 60606

EXAMINER	
BARTON, JONATHAN A	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,164	DESAI, KIRAN R.	
	Examiner	Art Unit	
	Jonathan Barton	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-28* is/are allowed.

6)☒ Claim(s) *1-23,29,31 and 32* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

a. Claims 1 and 4 are rejected under 35 U.S.C. 101 because the second cache is placed enhanced exclusive state every time it is written too, even though the enhanced exclusive state indicates information about the first cache that will not necessarily be true every time the secondary cache is written to. Added clarity is needed to indicate when the second cache will be placed in an enhanced exclusive state.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

b. Claim 32 recites the limitation "a second snoop hit-modified signal" in the third line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Albonesi et al (US 5113,514).

c. As for claims 1 and 4 Albonesi discloses

i. A first cache memory [claim 4] (Fig. 2 Item 28, Col. 5 Lines 46-50);

ii. A second cache memory [claim 4] (Fig. 2 Item 32, Col. 5 Lines 46-50);

iii. A processor operatively coupled to the first cache memory and the second cache memory [claim 4] (Fig. 2 Item 22, Col. 5 Lines 44-46); the processor

iv. Executing a store operation that hits a cache line in a second cache (Col. 3 Lines 37-43);

v. Placing the cache line in the second cache in an enhanced exclusive state indicating a copy of the cache line is in a first cache in a modified state (Col. 9 Lines 7-13 – Albonesi calls this a modified state, but its function is equivalent to applicant's enhanced exclusive state).

d. As for claims 2 and 5 Albonesi discloses

vi. The first cache comprises an L1 cache and the second cache comprises an L2 cache (Col. 5 Lines 46-50).

e. As for claims 3 and 6 Albonesi discloses

vii. Placing the cache line in the second cache in an enhanced modified state, the enhanced modified state indicating the copy of the cache lines may be in the first cache (Col. 9 Lines 4-7 – Albonesi calls this a private state, but its function is equivalent to applicant's enhanced modified state).

5. Claims 7, 11 –13 are rejected under 35 U.S.C. 102(b) as being anticipated by Merrell et al. (US 5,829,038).

f. As for claim 7 Merrell et al. disclose

viii. Issuing an inquiry to a first cache if the cache is in a predetermined state (Col. 3 Lines 60-62);

ix. Receiving a response to the inquiry if the cache line is in the predetermined state (Col. 3 Lines 62-65); and

x. Victimizing the cache line in the second cache without a write-back of the cache line from the second cache if the response is indicative of a cache hit (Col. 3 Lines 65-67).

g. As for claim 8 Merrell et al. disclose

xi. The first cache is an L1 cache and the second cache is an L2 cache (Col. 2 Line 66 – Col. 3 Line 7).

h. As for claim 11 Merrell et al. disclose

xii. The inquiry comprises an internal inquiry (Fig. 1 – in Fig. 1 it is seen that the processor which makes an inquiry is connected directly to the cache status memory [item 30] and is internal to the system).

i. As for claim 12 Merrell et al. disclose

xiii. Performing a write-back of the cache line from the second cache if the response is indicative of a cache miss (Col. 4 Lines 9-14).

j. As for claim 13 Merrell et al. disclose

xiv. Victimizing the cache line from the second cache after performing the write-back if the response is indicative of a cache miss (Col. 4 Lines 1-14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 9-10, 14-23, 29, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrell et al. (US 5,829,038) in view of Albonesi et al. (US 5,113,514).

k. As for claim 9 Merrell et al. disclose the depended upon claim 7 while Albonesi et al. teach

xv. The predefined state comprises an enhanced modified state indicating a copy of the cache line may be in the first cache (Col. 9 Lines 4-7).

xvi. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the enhanced modified state (private state) of Albonesi et al. with the cache coherency system of Merrell et al. because both systems are cache coherency systems relying on state information in order to maintain coherency and the enhanced modified state (private state) gives more detailed information about the overall status of the cache hierarchy and therefore provides a more exact data to base coherency maintenance actions on.

l. As for claim 10 Merrell et al. disclose

xvii. Performing a write-back of the cache line from the second cache without issuing the inquiry to the first cache if the cache line is in a non [predefined] state (Col. 4 Lines 9-14).

xviii. Albonesi et al. teach that the "non [predefined] state" is in fact a "non-enhanced modified state" (Col. 9 Lines 4-7).

m. As for claim 14 Albonesi et al. teach

xix. Victimizing the cache line in the second cache without issuing the inquiry to the first cache if the cache line is in an enhanced exclusive state indicating a copy of the cache line is in the first cache (Col. 10 Lines 24-30).

n. As for claim 15 Merrell et al. disclose

xx. Victimizing the cache line in the second cache comprises victimizing the cache line in the second cache without performing a write-back of the cache line from the second cache (Col. 3 Lines 62-67).

o. As for claim 16 Albonesi et al. teach

xxi. The enhanced exclusive state indicates the copy of the cache line in the first cache is in a modified state (Col. 9 Lines 4-7).

p. As for claim 17 Merrell et al. disclose

xxii. A first cache memory (Fig. 1 L1 cache, Col. 3 Lines 1-7);

xxiii. A second cache memory operatively coupled to the first cache memory (Fig. 1 L2 cache, Col. 3 Lines 1-7),

xxiv. The second cache memory being structured to issue an inquiry to the first cache memory if a cache line to be victimized in the second cache memory is in an [predefined] state (Col. 3 Lines 60-67), while

q. Albonesi et al. teach

xxv. The [predefined] state is an enhanced modified state (Col. 9 Lines 4-7), and

xxvi. The enhanced modified state indicating a copy of the cache line may be in the first cache memory (Col. 9 Lines 4-7).

r. As for claim 18 Merrell et al. disclose

xxvii. The first cache memory is an L1 cache and the second cache memory is an L2 cache (Fig. 1 L1 and L2 caches, Col. 3 Lines 1-7).

s. As for claim 19 Merrell et al. disclose

xxviii. A main memory operatively coupled to the second cache memory (Fig. 1 Item 60 Col. 3 Lines 5-7), wherein the second cache memory is structured to:

xxix. Receive a response to the inquiry (Col. 3 Lines 60-62); and

xxx. Victimize the cache line in the second cache memory without a write-back of the cache line to the main memory if the response is indicative of a cache hit (Col. 3 Lines 62-67).

t. As for claim 20 Albonesi et al. teach

xxxi. The second cache memory is structured to perform the write-back of the cache line without issuing the inquiry to the first cache memory if the cache line is not in the enhanced modified state (Col. 10 Lines 24-30).

u. As for claim 21 Albonesi et al. teach

xxxii. The second cache memory performs the write-back of the cache line if the response is indicative of a cache miss (Col. 10 Lines 24-30).

v. As for claim 22 Albonesi et al. teach

xxxiii. The second memory is structured to victimize the cache line in the second cache after performing the write-back if the response is indicative of a cache miss (Col. 10 Lines 24-30).

w. As for claim 23 Albonesi et al. teach

xxxiv. The second cache memory is structured to victimize the cache line in the second cache memory without issuing the inquiry to the first cache memory if the cache line is in an enhanced exclusive state indicating a

copy of the cache line is in the first cache memory in a modified state (Col. 10 Lines 24-30, Col. 9 Lines 7-13).

x. As for claim 29 Merrell et al. disclose

xxxv. A processor (Fig. 1 Item 10 Col. 2 Lines 55-64);

xxxvi. A first cache operatively coupled to the processor (Fig. 1 L1 cache, Col. 3 Lines 1-7); and

xxxvii. A second cache operatively coupled to the processor (Fig. 1 L2 cache, Col. 3 Lines 1-7),

xxxviii. The second cache being structured to post a snoop hit signal if a cache line in the second cache is in one of an [predefined set of states] (Col. 3 Lines 60-63),

y. Albonesi et al. teach

xxxix. The [predefined set of states] is an exclusive state, an enhanced exclusive state, and a shared state (Col. 8 Line 64 – Col. 9 Line 13), and

xl. wherein the enhanced exclusive state indicates a modified copy of the cache line is in the first cache (Col. 9 Lines 7-13).

z. As for claim 31 Merrell et al. disclose

xli. The first cache memory comprises an L1 cache and the second cache memory comprises an L2 cache (Fig. 1 L1 and L2 caches, Col. 3 Lines 1-7).

Allowable Subject Matter

8. Claims 24-28 are indicated as allowable over the prior art.

9. Claims 30 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim 32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

aa. Claims 24 and 30 contain at least the following allowable subject matter:

xlii. Posting at least a first snoop hit-modified signal if the cache line in the second cache is in one of a modified state and an enhanced modified state, wherein the enhanced modified state indicates an updated copy of the cache line may be in the first cache.

bb. Claim 32 contains at least the following allowable subject matter:

xliii. The second cache is structured to: detect a second snoop hit-modified signal from the first cache; and invalidate the cache line in the second cache in response to detecting the second snoop hit-modified signal from the first cache.

cc. Claims 25-28 depend from claim 24 and therefore contain its allowable subject matter.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

dd. Arimilli et al. (US 6,292,872)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Barton whose telephone number is 571-272-8157. The examiner can normally be reached on Monday - Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Barton
Examiner
Art Unit 2186

JB

MATTHEW D. ANDERSON
PRIMARY EXAMINER